**ECE 429 Lab 2**

**Inverter Schematic and Simulation**

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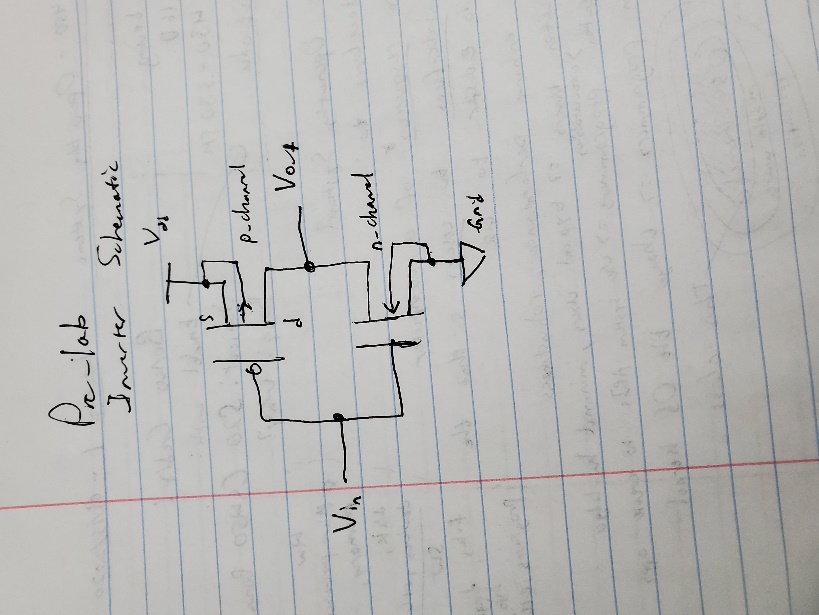
**Introduction**

The objective of this lab is to use VLSI design to design and test an inverter schematic design. A secondary objective is to become more familiar with the VSLI program, as the lab manual is a tutorial.

**Theory/Pre-Lab**

It is costly to manufacture VLSI chips, and it is difficult to test nanoscale devices. As a result, designers rely on computer-aided design (CAD) to test and validate designs before taping-out and silicon debugging. This lab will introduce the Cadence Virtuoso platform, which is one of the most widely used electronic design automation platforms. Virtuoso will be used to design a transistor level schematic of an inverter while the design will be tested with a SPICE simulation.

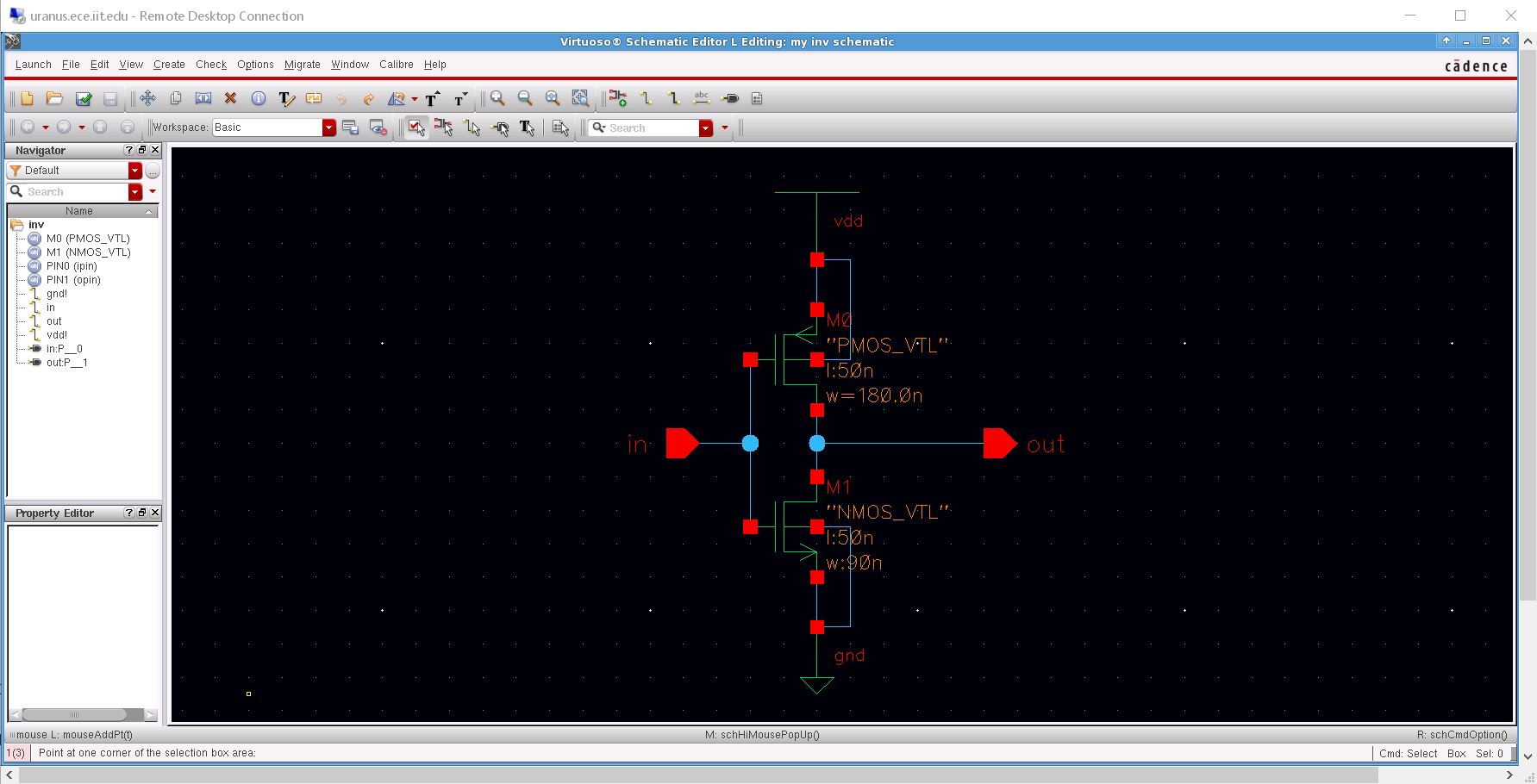
As a part of the pre-lab, Tutorial I: Inverter Schematic and Simulation was read. A schematic for the static CMOS inverter was also made:

Figure 1: Inverter Transistor-Level Schematic

**Implementation**

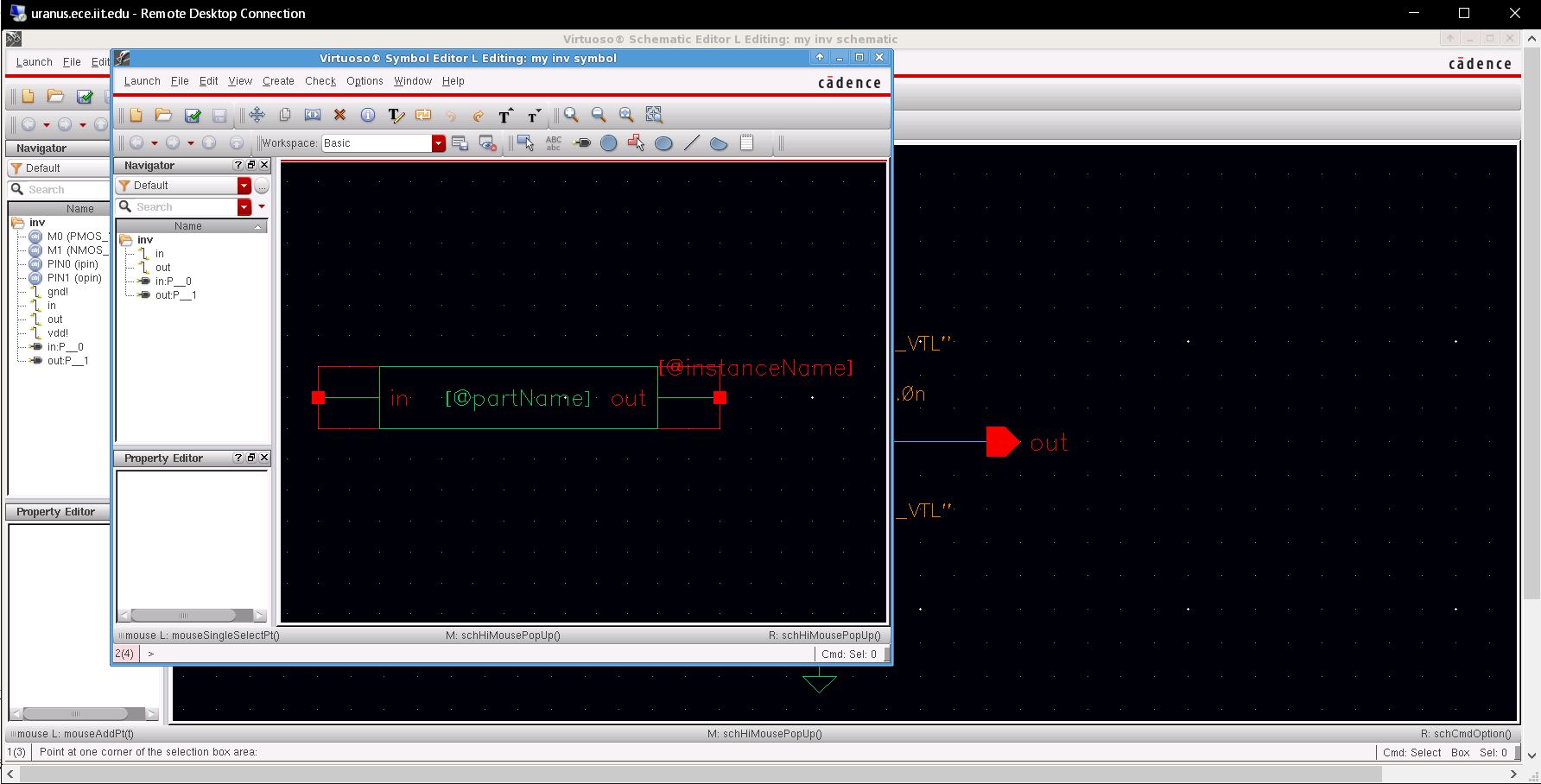
Following the Inverter Schematic from the Pre-Lab, the following schematic was made in Cadence Virtuoso:

Figure 2: VLSI Inverter Schematic



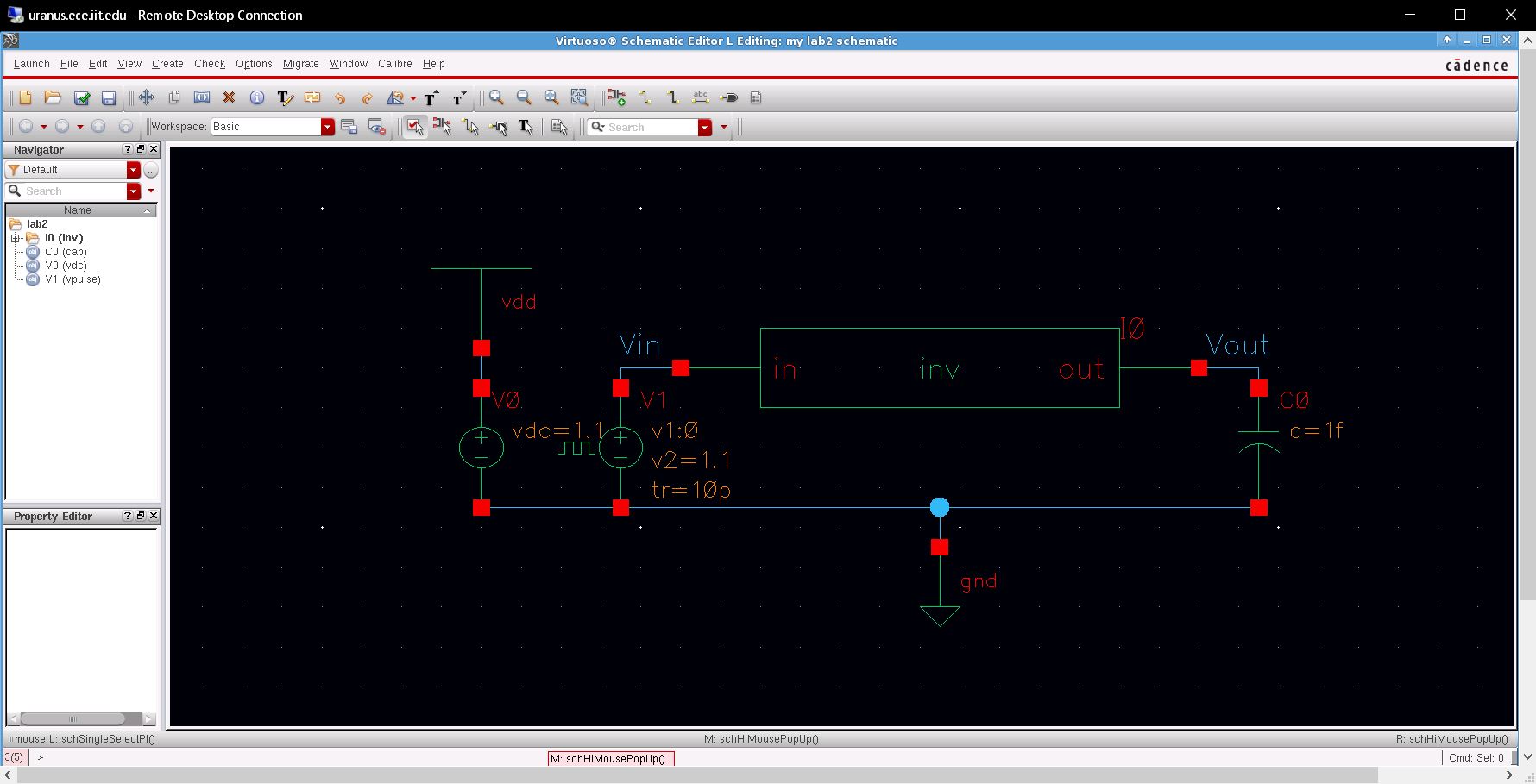
The body of the PMOS transistor is located next to the Vdd. In the schematic, it is above the NMOS transistor that is next to the Ground. The PMOS transistor has a width of 180 nm while the NMOS transistor has a width of 90 nm. Both transistors have a length of 50 nm.

Although the schematic was successfully created, it could not interact with other components to form a circuit. As such, the Inverter was converted to a symbol:

Figure 3: Inverter Symbol

The symbol was then utilized into a circuit:

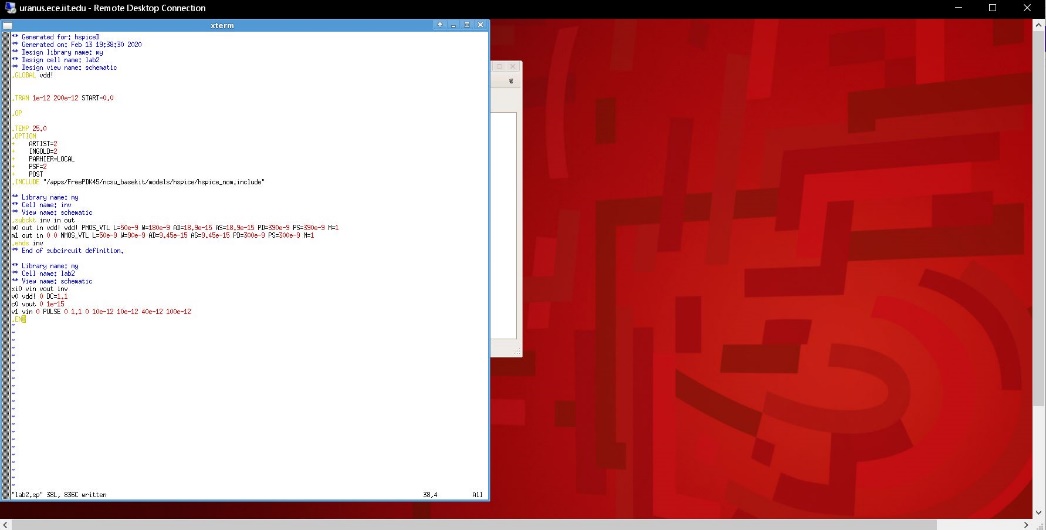
Figure 4: Circuit Schematic



The supply voltage is at 1.1 V for the test circuit. Rise Time (and, conversely, Fall time) refers to the time it takes for the voltage pulse to go from the minimum voltage to the maximum voltage. Pulse width refers to the amount of time the voltage pulse is high/low before falling/rising again.

Now that the circuit was created, it was formatted into a Spice Netlist for simulation purposes:

Figure 5: Spice Netlist



With the netlist created, HSPICE was used to output a .tr0 file, which could be run with Cosmos Scope. CScope outputs a graph of Voltage (V) vs Time (s) for both Vin and Vout, the voltage going into the inverter and coming out, respectively. The delay could be measured using a measuring tool within the program.

Figure 6: CScope Plot and measurements

The delay came out to be about 7.14 ps, which, according to the tutorial manual, seems to be within the expected results. The maximum rising delay from the Tutorial shows 7.1892 ps, which is about 7.19 x (10-12) seconds.

In order to obtain an inverter design with equal rising and falling delays, the PMOS transistor would need to become smaller.

**Conclusion**

In conclusion, this lab seems to be a success. The results were all as they were expected to be and there were no difficulties. As for the secondary objective, this lab did make me more familiar with VLSI design, but there are still moments where I am unclear as to what I am doing (for example, creating the Netlist). Hopefully, the next few labs get me more familiar with the programs.